In re Patent Application of:
ENRIQUEZ ET AL
Serial No. **10/091976**
Filing Date: **MARCH 6, 2002**

REMARKS

By the present amendment Applicants have endeavored to more concisely define the subject manner of the present invention in a manner which is believed to be neither disclosed nor suggested by the prior art of record, in particular that cited in the statement of the final rejection of June 13, 2005.

Of the replacement claims 36-58, claim 36 is independent and claims 37-58 depend upon claim 36. Claim 36 is believed to particularly point out and distinctly claim the subject matter for which patent protection is sought in a manner that clearly patentably distinguishes the subject invention from the CODEC and SLIC circuit arrangements of the prior art cited in the Office Action of June 13, 2005.

In order to gain an appreciation for the differences between the invention claimed in replacement claims 36-58 and the prior art cited in the Office Action of June 13, 2005, the present invention will be briefly reviewed. To this end, attention is directed to Figure 1 of the drawings of the present application which shows the overall architecture of the invention. The subscriber line interface circuit according to the subject invention includes two portions: 1)-- a high voltage portion which interfaces with the subscriber line pair, shown in the majority of the left hand portion of Figure 1, and 2) -- a low voltage portion shown at 200 in the right hand portion of Figure 1. The high voltage analog section as described and claimed has no intelligence of its own, but is configured to perform analog (voice, ringing, etc.) signal processing and interface functions of a conventional SLIC based upon control inputs and programmed parameters of signal section 200 as described in paragraph [19] on page 9 of the specification. The mixed signal section 200

includes two components. One is a digital signal process-based CODEC 200C which interfaces voice and ringing signals with the high voltage section. In addition to the CODEC, the mixed signal section includes a supervisory microcontroller subsection 200S, which, as described in paragraph [20] on page 9 of the present specification, may comprise a conventional microprocessor and associated memory, and is programmable to establish parameters and to control the operation of the high voltage section. As is further described in paragraph [23] on page 11 of the specification, the supervisory microcontroller subsection 200S defines respective values of bias currents for application to various ones of the functional blocs or units of the high voltage section 100, with the values being supplied to the high voltage section by way of digital control signals that are latched in a control and latch interface unit 190. From this unit, current signals, the values of which have been programmed by the supervisory microcontroller, are distributed to current generators throughout the high voltage section so as to controllably establish or define the operational parameters of the various analog circuits of the high voltage section.

Newly presented independent claim 36, upon which claims 37-58 depend, is believed to concisely define the architecture of the SLIC described above and shown in Figure 1. As a first component, the SLIC comprises a high voltage analog section containing analog operational circuits, operational parameters of which are programmable in accordance with respective bias currents supplied thereto, and to which power sufficient for any signalling conditions of tip and ring conductors of a respective subscriber loop pair is supplied. The analog operational circuits are operative to drive the tip and ring conductors of the respective subscriber loop pair in accordance with analog input and analog control signals supplied thereto.

A second component of the SLIC of claim 36 is a low voltage digitally programmable signal generation and digital signal processing section. This section is operative to interface voice and ringing signals with the analog circuits of the high voltage section and to monitor and control operational characteristics of the analog circuits of the high voltage section. According to the definition of the SLIC in claim 36, the low voltage digitally programmable signal generation and digital signal processing section includes two subcomponents. The first is s digital signal processor (DSP)-based CODEC. This CODEC is operative to interface voice and ancillary signals with analog circuits of the high voltage analog section. A second component of the low voltage digitally programmable signal generation and digital signal processing section is a supervisory digital signal processor that is separate from the CODEC. This processor is operative to program respective values of bias currents that control operational parameters of respective ones of the analog operational circuits, the bias currents as programmed by the supervisory digital signal processor being coupled to the analog operational circuits, thereby establishing the programmable operational parameters thereof.

New claim 37, which depends upon claim 36, specifies that the high voltage section includes a control and latch interface unit. As described above, this corresponds to the control and latch interface unit 190 which is operative to receive and store from the supervisory digital processor a plurality of digital input signals for defining values of the bias currents to which operational parameters of respective ones of the analog operational circuits of the high voltage section are established. Again, this is described in paragraph [23] on page 11 of the present specification.

Newly presented claim 38 depends upon claim 36 and further

delimits claim 36 by the subject matter of previously filed original claim 3.

Claims 39-58 essentially correspond to the subject matter defined in original claims 4-23, but with specificity in distinguishing between whether the signals being supplied to the high voltage section are derived from the CODEC, or whether they are derived from the supervisory digital signal processor, which is separate from the CODEC.

Looking now at the prior art cited in the outstanding Office Action, the patent to Caine et al 6,735,302 discloses a SLIC assembly 100 in combination with a CODEC 102. The CODEC 102 is operative to interface voice and data and associated control signals with the SLIC as shown, for example, in Figures 3, 7 and 8 of the patent.

Upon comparing, or more correctly contrasting the invention defined in claims 36-58 with what is disclosed by Caine et al, several differences become immediately apparent.

A first and major distinction between Applicants' claimed invention and the CODEC/SLIC architecture of Caine et al is the fact that Caine et al employs no separate supervisory control processor separate from the CODEC 102, which is operative to program respective values of bias currents that control operational parameters of respective ones of the analog operational circuits of the high voltage, as defined in the last clause of claim 36. Caine et al simply disclose the combination of a CODEC and a SLIC. Applicants' invention is the architecture of a SLIC, which includes the particularly high defined voltage section, and a multiple component low voltage digitally programmable signal generation and digital signal processing section, that includes both a CODEC and a separate supervisory

digital signal processor that is operative to program respective values of bias currents for establishing the programmable operational parameters of the analog circuits of the high voltage section. No corresponding circuitry is disclosed or suggested by Caine et al, so the patent does not support a rejection of claims 36-58 either under 35 U.S.C. § 102 or 35 U.S.C. § 103.

The patent to Rosenbaum et al 5,323,461 discloses a two-wire telephone line interface circuit that includes a switching circuit and a controlled voltage generator which are respectively controlled by a control circuit. The control circuit controls the switching circuit to supply a supply voltage for it and associated driver circuit that feeds the switching circuit. The control circuit also controls the switching circuit to selectively supply the controlled output voltage of the voltage generator as a signaling voltage for high voltage signaling, such as ringing, on the line.

Applicants' review of the patent to Rosenbaum et al fails to reveal the combination of features set forth in claim 36, discussed at length above. There is neither a high voltage analog section whose analog operational circuits have their parameters programmable in accordance with respective bias currents, nor is there a low voltage digitally programmable signal generation and digital signal processing section that includes both a CODEC and a separate supervisory digital signal processor that programs respective values of the bias currents for controlling operational characteristics of the analog circuits of the high voltage section as discussed previously.

The patent to Burke et al 6,453,040 has been cited because it shows within an adaptor module, such as adaptor modules 41, 42, 43 and 44, the combination of a SLIC and a CODEC. In effect, Burke et al show what is already shown in Caine et al by the

combination of a CODEC 112 and a SLIC 113. Applicants' review of the patent to Burke et al has failed to uncover the combination of features defined in claim 36, upon which claims 37-58 depend. There is no high voltage section containing analog operational circuits that are programmable in accordance with respective bias currents supplied thereto by a supervisory digital signal processor that is separate from the CODEC.

The tertiary patent to Chea 4,315,106 is directed to a current regulation circuit for supplying regulated current to a two-wire analog subscriber line. Chea employs a pair of line feed impedance elements of substantially the same magnitude, a differential amplifier, a reference voltage source, a summing circuit and a circuit for providing a signal indicative of the line current. The combination of features called for in claim 36 is not shown or suggested by Chea and the patent to Chea contains no disclosure or suggestion of somehow modifying the circuits of the other patents discussed above, to result in a configuration upon which Applicants' claims would read.

In summary, Applicants' claimed invention is not simply the combination of analog circuits of a SLIC and an associated CODEC, something which is disclosed by both Caine et al and Burke et al. Applicants' invention is directed to a combination of features which define a new architecture for a SLIC, per se. This combination of features requires a high voltage section containing analog operational circuits whose operational parameters are programmable in accordance with respective bias currents supplied thereto. Associated with the high voltage section is a low voltage section that is operative to interface voice and ringing signals with the analog circuits and to monitor and control operational characteristics thereof, the low voltage section including a CODEC on the one hand, and a supervisory digital signal processor on the other, which is separate from the

CODEC, and which is operative to program respective values of the bias currents that control operational parameters of respective ones of the analog circuits so as to establish the programmable operational parameters thereof. These various bias currents are shown at the output of the bias_control portion of the latch unit 190 in Figure 3 of the drawings of the present application and are distributed throughout the analog circuitry of Figures 2 and 3 to control the operational parameters thereof. There is no disclosure or suggestion of this architecture or functionality in the prior art cited in the Office Action of June 13, 2005.

As a consequence, it is respectfully submitted that claims 36-58 submitted with this amendment patentably distinguish over the prior art cited in the Office Action of June 13, 2005 and are thus in condition for allowance.

In view of the foregoing amendments and remarks, favorable reconsideration of this application and a Notice of Allowability of replacement claims 36-58 are earnestly solicited.

Of course, if the Examiner is of the opinion that additional minor amendments to the claims are in order, he is respectfully invited to contact the undersigned attorney at the telephone number listed below so that any such changes may be discussed and, where warranted, effected.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **703-872-9306** to the COMMISSIONER FOR PATENTS, this 26 day of August 2005.